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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,557	08/26/2003	Hyung-Seok Kim	SAM-0437	5509

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EXAMINER

PIZIALI, JEFFREY J

ART UNIT	PAPER NUMBER
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2629

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/649,557

Applicant(s)

KIM, HYUNG-SEOK

Examiner

Jeff Piziali

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-20 is/are rejected.
- 7) ☒ Claim(s) 4 and 5 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 February 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed (on 14 September 2006) in this application after final rejection (mailed 11 May 2006). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11 August 2006 has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings were received on 21 February 2006. These drawings are acceptable.

Claim Objections

4. Claims 4 and 5 are objected to because of the following informalities: Both claims 4 and 5 are improperly dependent upon canceled claim 2. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 3-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyazaki (US 2002/0154080 A1).

Regarding claim 1, Miyazaki discloses a liquid crystal display driver (see Paragraph 2) comprising: a driving voltage generating circuit [Fig. 1B; 121] for generating first through fifth driving voltages [Fig. 8; V1, V2=V82, V3, V4, and V5] and outputting the generated voltages via first through fifth output terminals [Fig. 8; V1, V2=V82, V3, V4, and V5]; a common/segment driving circuit [Fig. 2; 221 and 222], controlled by a driving polarity signal [i.e. frame signal] that is applied to the common/segment driving circuit, for receiving the first through fifth driving voltages to generate a common driving signal [i.e. com output] and a segment driving signal [i.e. seg output] (see Paragraphs 38-40); a first capacitor [Fig. 8; C0] connected between the first output terminal and a ground voltage; a second capacitor [Fig. 8; C4]; a third capacitor [Fig. 8; C3]; and a control circuit comprising a plurality of switches [Fig. 8; SW1-SW3] for controlling connection of the output terminals and the capacitors in response to the driving polarity signal (see Paragraphs 73-75), wherein each switch of the plurality of switches is controlled by the driving polarity signal (see Paragraphs 60-62), and wherein the capacitors are selectively connected to driving voltages used by the common/segment driving

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circuit, but not to driving voltages not used by the common/segment driving circuit, according to a logic state of the driving polarity signal (see Paragraphs 63-64); and wherein the control circuit comprises:

a first switch [Fig. 8; SW3] for connecting one end of the second capacitor [Fig. 8; right end] in a first position of the first switch [Fig. 8; SW3b] to the first output terminal [Fig. 8; V1] and in a second position of the first switch [Fig. 8; SW3a] to the fifth output terminal [Fig. 8; V5] in response to the driving polarity signal;

a second switch [Fig. 8; SW2] for connecting the other end of the second capacitor [Fig. 8; left end] in a first position of the second switch [Fig. 8; SW2b] to the second output terminal [Fig. 8; V2] and in a second position of the second switch [Fig. 8; SW2a] to the ground voltage [Fig. 8; at SW1a] in response to the driving polarity signal;

a third switch [Fig. 8; SW1] for connecting one end of the third capacitor [Fig. 8; right end] in a first position of the third switch [Fig. 8; SW1b] to the second output terminal [Fig. 8; V2 via SW2b] and in a second position of the third switch [Fig. 8; SW1a] to the fourth output terminal [Fig. 8; V4] in response to the driving polarity signal; and

a fourth switch [Fig. 8; SW2] for connecting the other end of the third capacitor [Fig. 8; left end] in a first position of the fourth switch [Fig. 8; SW2a] to the third output terminal [Fig. 8; V3 via SW1b] and in a second position of the fourth switch [Fig. 8; SW2b] to the fifth output terminal [Fig. 8; V5] in response to the driving polarity signal (see Paragraphs 73-75).

Regarding claim 3, Miyazaki discloses the common/segment driving circuit generates the common driving signal [Fig. 6; COM4] and the segment driving signal [Fig. 6; SEGn] using the

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first driving voltage, the fourth driving voltage, the fifth driving voltage, and the ground voltage when the driving polarity signal is in a first logic state [Fig. 6; Frame 1], and generates the common driving signal and the segment driving signal using the first driving voltage, the second driving voltage, the third driving voltage, and the ground voltage when the driving polarity signal is in a second logic state [Fig. 6; Frame 2] (see Paragraphs 59-69).

Regarding claim 4, Miyazaki discloses when the driving polarity signal is in the first logic state, one end of the second capacitor is coupled to the fifth output terminal by the first switch [Fig. 8; SW2a], the other end of the second capacitor is coupled to the ground voltage by the second switch [Fig. 8; SW3a], one end of the third capacitor is coupled to the fourth output terminal by the third switch [Fig. 8; SW1a], and the other end of the third capacitor is coupled to the fifth output terminal by the fourth switch [Fig. 8; SW2a] (see Paragraphs 73-75).

Regarding claim 5, Miyazaki discloses when the driving polarity signal is in the second logic state, one end of the second capacitor is coupled to the first output terminal by the first switch [Fig. 8; SW3b], the other end of the second capacitor is coupled to the second output terminal by the second switch [Fig. 8; SW2b], one end of the third capacitor is coupled to the second output terminal by the third switch [Fig. 8; SW1b], and the other end of the third capacitor is coupled to the third output terminal by the fourth switch [Fig. 8; SW1b] (see Paragraphs 73-75).

Regarding claim 6, Miyazaki discloses the voltage difference between every two adjacent driving voltages among the first through fifth driving voltages is the same (see Paragraphs 52-53).

Regarding claim 7, Miyazaki discloses the common/segment driving circuit comprises: a common driving circuit [Fig. 2; 221], controlled by the driving polarity signal, for receiving the first driving voltage, the second driving voltage, the fifth driving voltage, and the ground voltage to generate the common driving signal; and a segment driving circuit [Fig. 2; 222], controlled by the driving polarity signal, for receiving the first driving voltage, the third driving voltage, the fourth driving voltage, and the ground voltage to generate the segment driving signal (see Paragraphs 38-40).

Regarding claim 8, Miyazaki discloses the common driving signal [Fig. 6; COM4] has the first driving voltage level and the fifth driving voltage level when the driving polarity signal is in a first logic state [Fig. 6; Frame 1], and has the second driving voltage level and the ground voltage level when the driving polarity signal is in a second logic state [Fig. 6; Frame 2] (see Paragraphs 59-68).

Regarding claim 9, Miyazaki discloses the segment driving signal [Fig. 6; SEGn] has the fourth driving voltage and the ground voltage when the driving polarity signal is in a first logic state [Fig. 6; Frame 1], and has the first driving voltage and the third driving voltage when the driving polarity signal is in a second logic state [Fig. 6; Frame 2] (see Paragraphs 59-68).

Regarding claim 10, this claim is rejected by the reasoning applied in rejecting claim 1.

Regarding claim 11, this claim is rejected by the reasoning applied in rejecting claim 3.

Regarding claim 12, this claim is rejected by the reasoning applied in rejecting claim 4.

Regarding claim 13, this claim is rejected by the reasoning applied in rejecting claim 5.

Regarding claim 14, this claim is rejected by the reasoning applied in rejecting claim 6.

Regarding claim 15, this claim is rejected by the reasoning applied in rejecting claim 7.

Regarding claim 16, this claim is rejected by the reasoning applied in rejecting claim 8.

Regarding claim 17, this claim is rejected by the reasoning applied in rejecting claim 9.

Regarding claim 18, this claim is rejected by the reasoning applied in rejecting claims 1, 4, and 5.

Regarding claim 19, this claim is rejected by the reasoning applied in rejecting claim 3.

Regarding claim 20, this claim is rejected by the reasoning applied in rejecting claim 6.

Response to Arguments

7. Applicant's arguments filed 11 August 2006 have been fully considered but they are not persuasive.

The applicant contends the cited prior art of Miyazaki (US 2002/0154080 A1) neglects teaching: a first switch for connecting one end of the second capacitor in a first position of the first switch to the first output terminal and in a second position of the first switch to the fifth output terminal in response to the driving polarity signal; a second switch for connecting the other end of the second capacitor in a first position of the second switch to the second output terminal and in a second position of the second switch to the ground voltage in response to the driving polarity signal; a third switch for connecting one end of the third capacitor in a first position of the third switch to the second output terminal and in a second position of the third switch to the fourth output terminal in response to the driving polarity signal; and a fourth switch for connecting the other end of the third capacitor in a first position of the fourth switch to the third output terminal and in a second position of the fourth switch to the fifth output terminal in response to the driving polarity signal (see Paragraphs 73-75). (see Pages 10-12 of the 'Amendment After Final Rejection' filed 11 August 2006). However, the examiner respectfully disagrees.

Miyazaki does indeed disclose a first switch [Fig. 8; SW3] for connecting one end of the second capacitor [Fig. 8; right end] in a first position of the first switch [Fig. 8; SW3b] to the first output terminal [Fig. 8; V1] and in a second position of the first switch [Fig. 8; SW3a] to the

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fifth output terminal [Fig. 8; V5] in response to the driving polarity signal; a second switch [Fig. 8; SW2] for connecting the other end of the second capacitor [Fig. 8; left end] in a first position of the second switch [Fig. 8; SW2b] to the second output terminal [Fig. 8; V82] and in a second position of the second switch [Fig. 8; SW2a] to the ground voltage [Fig. 8; at SW1a] in response to the driving polarity signal; a third switch [Fig. 8; SW1] for connecting one end of the third capacitor [Fig. 8; right end] in a first position of the third switch [Fig. 8; SW1b] to the second output terminal [Fig. 8; V82 via SW2b] and in a second position of the third switch [Fig. 8; SW1a] to the fourth output terminal [Fig. 8; V4] in response to the driving polarity signal; and a fourth switch [Fig. 8; SW2] for connecting the other end of the third capacitor [Fig. 8; left end] in a first position of the fourth switch [Fig. 8; SW2a] to the third output terminal [Fig. 8; V3 via SW1b] and in a second position of the fourth switch [Fig. 8; SW2b] to the fifth output terminal [Fig. 8; V5] in response to the driving polarity signal (see Miyazaki: Paragraphs 73-75).

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Jeff Piziali
27 November 2006